

18 October 2023

To Whom It May Concern

## Global Tender for thin-film Piezoelectric (AlN/AlScN) deposited on Metallized Silicon and SOI wafers

This is an RFQ (Request for Quote) for procurement of Piezoelectric thin-film deposited on Silicon and SOI wafers for Centre for Nano Science and Engineering (CeNSE) at IISc, Bangalore.

CeNSE is a multidisciplinary research department at IISc that houses a 14,000 sq. ft. cleanroom and characterization facility used by more than 50 faculty members from various disciplines at IISc.

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|---|-----------|----------------|---|
| 1 | Section 1 | Bid Schedule   |   |
| 2 | Section 2 | Eligibility    | As specified by IISc                              |
|   |           | Criteria       |   |
| 3 | Section 3 | Terms and      | As specified by IISc                              |
|   |           | Conditions     |   |
| 4 | Section 4 | Specifications | Technical specifications                          |
| 5 | Section 5 | Technical Bid  | Annexure 1: Bidder details                        |
|   |           |                | Annexure 2: Declaration regarding experience of   |
|   |           |                | bidder  |
|   |           |                | Annexure 3: Declaration regarding clean track     |
|   |           |                | record of the bidder                              |
|   |           |                | Annexure 4: Declaration of acceptance of tender   |
|   |           |                | Annexure 5: Terms and conditions. Details of      |
|   |           |                | item quoted                                       |
| 6 | Section 6 | Commercial     | Quotation with Price, Technical specifications of |
|   |           | Bid            | the equipment                                     |
| 7 | Section 7 | Check List     |   |



## Section 1 - Bid Schedule

| 1 | Tender No                  |   |  |  |  |
|---|----------------------------|---|--|--|--|
| 2 | Tender Date                | 18 October 2023                               |  |  |  |
| 3 | Item Description           | Procurement of thin-film Piezoelectric        |  |  |  |
|   | _                          | (AlN/AlScN) deposited on Metallized Silicon   |  |  |  |
|   |                            | and SOI wafers                                |  |  |  |
| 4 | Tender Type                | Two bid system                                |  |  |  |
|   |                            | (i) Technical Bid (Part A)                    |  |  |  |
|   |                            | (ii) Commercial Bid (Part B)                  |  |  |  |
|   |                            |   |  |  |  |
| 5 | Place of tender submission | Chairperson Office                            |  |  |  |
|   |                            | First Floor                                   |  |  |  |
|   |                            | Centre for Nano Science and Engineering       |  |  |  |
|   |                            | Indian Institute of Science, Bangalore 560012 |  |  |  |
| 6 | Last Date & Time for       | 15 November 2023                              |  |  |  |
|   | submission of tender       |   |  |  |  |
| 7 | For further clarification  | Dr. Gayathri Pillai                           |  |  |  |
|   |                            | Room No: FF05                                 |  |  |  |
|   |                            | Centre for Nano Science and Engineering       |  |  |  |
|   |                            | Indian Institute of Science, Bangalore, India |  |  |  |
|   |                            | 560012.                                       |  |  |  |
|   |                            | Office: +91-80-2293-3250                      |  |  |  |
|   |                            | E-mail: gpillai@iisc.ac.in                    |  |  |  |



## <u>Section 2 – Eligibility Criteria</u>

## Prequalification criteria:

- The Bidder's firm should have existence for a minimum of 3 years. (Enclose 1. Company Registration Certificate)
- This tender is open to all global Original Wafer Manufacturers and Commercial Thin-Film Deposition Facility Providers or their Indian-authorized distributor
- The bidder should sign and submit the declaration for Acceptance of Terms and Conditions as per -Annexure 4.
- The Bidder must not be blacklisted/banned/suspended or have a record of any service-related dispute with any organization in India or elsewhere. A declaration to this effect has to be given as per Annexure 3.



## **Section 3 – Terms and Conditions**

#### A) Submission of Tender:

- 1.All documentations in the tender should be in English.
- 2. Tender should be submitted in two envelops (two bid system).
- a. Technical Bid (Part-A) Technical bid consisting of all technical details and check list for conformance to technical specifications.

The technical proposal should contain a technical compliance table with 5 columns.

- i. The first column must list the technical requirements, in the order that they are given in the technical requirement below.
- ii. The second column should provide specifications of the wafer against the requirement. Please provide quantitative responses wherever possible.
- iii. The third column should describe your compliance with a "Yes" or "No" only. Ensure that the entries in column 2 and column 3 are consistent.
- iv. The fourth column should state the reasons/explanations/context for deviations, if any.
- v. The fifth column can contain additional remarks from the original supplier. You can use this opportunity to highlight technical features, qualify response of previous columns, or provide additional details, compare your solution with that of your competitors or provide details as requested in the technical requirements table below.
- b. Commercial Bid (Part-B) Indicating item wise price for the items mentioned in the technical bid, as per the format of quotation provided in tender, and other commercial terms and conditions.
- 3.The technical bid and price bid should each be placed in separate sealed covers, superscripting on both the envelopes the tender no. and the due date. Both these sealed covers are to be placed in a bigger cover which should also be sealed and duly superscripted with the Tender No, Tender Description & Due Date.
- 4.The SEALED COVER superscripting tender number / due date & should reach Chairperson Office, Centre for Nanoscience and Engineering, Indian Institute of Science, Bangalore 560012, India on or before due date mentioned in the tender notice. In case due date happens to be holiday the tender will be accepted and opened on the next working day. If the quotation cover is not sealed, it will be rejected.
- 5.All queries are to be addressed to the person identified in "Section 1 Bid Schedule" of the tender notice.



6.GST/other taxes, levies etc., are to be indicated separately. The BIDDER should mention GST Registration and PAN in the tender document (Indian Bidders only).

7.If price is not quoted in Commercial Bid as per the format provided in tender document the bid is liable to be rejected.

8. The Institute reserves the right to accept or reject any bid and to annul the bidding process and reject all bids at any time prior to the award of contract, without there by incurring any liability to the affected bidder or bidders or any obligation to inform the affected bidder or bidders.

9.Incomplete bids will be summarily rejected.

- 10. Please specify 3 previous supplies made to facilities in India working on semiconductor applications.
- 11. The vendor should produce Bill of Entry.

#### **B)** Cancellation of Tender:

Notwithstanding anything specified in this tender document, IISc Bangalore, in its sole discretion, unconditionally and without having to assign any reason, reserves the rights:

- a. To accept OR reject lowest tender or any other tender or all the tenders.
- b. To accept any tender in full or in part.
- c. To reject the tender, offer not confirming to the tender terms.

#### C) Validity of the Offer:

The offer shall be valid 90 Days from the date of opening of the commercial bid.

#### **D)** Evaluation of Offer:

- 1. The technical bid (Part A) will be opened first and evaluated.
- 2. Bidders meeting the required eligibility criteria as stated in Section 2 of this document shall only be considered for Commercial Bid (Part B) opening. Further, agencies not furnishing the documentary evidence as required will not be considered.
- 3. Pre- qualification of the bidders shall not imply final acceptance of the Commercial Bid. The agency may be rejected at any point during technical evaluation or during commercial evaluation. The decision in regard to acceptance and / or rejection of any offer in part or full shall be the sole discretion of Purchase Committee IISc Bangalore, and the decision in this regard shall be binding on the bidders.
- 4. The award of the contract will be subject to acceptance of the terms and conditions stated in this tender.
- 5. Any offer which deviates from the vital conditions (as illustrated below) of the tender is liable to be rejected:



- a. Non-submission of complete offers.
- b. Receipt of bids after due date and time and or by email / fax (unless specified otherwise).
  - c. Receipt of bids in open conditions.
- 6. In case any BIDDER is silent on any clauses mentioned in these tender documents, Purchase Committee IISc Bangalore shall construe that the BIDDER had accepted the clauses as of the tender and no further claim will be entertained.
- 7. No revision in the terms and conditions quoted in the offer will be entertained after the last date and time fixed for receipt of tenders.
- 8. Lowest bid will be calculated based on the total price of all items tendered.

#### **H) Purchase Order:**

- 1. The order will be placed on the bidder whose bid is accepted by IISc based on the terms & conditions mentioned in the tender document.
- 2. The quantity of the items in tender is only indicative. Purchase Committee IISc, Bangalore reserves the right to increase /decrease the quantity of the items depending on the requirement.
- 3. If the quality of the product and service provided is not found satisfactory, Purchase Committee IISc, Bangalore reserves the right to cancel or amend the contract.

#### I) Delivery:

The bidder shall provide the lead time to delivery at IISc, Bangalore from the date of receipt of the purchase order. The items should be delivered within 90 days from the date of receipt of the purchase order. The supply of the items will be considered as effected only on satisfactory inspection at IISc, Bangalore. No partial shipment is allowed.

#### **J) Payment Terms:**

**Payment Terms:** 

The payment will be through a Letter of Credit and the milestone of the payment will be determined after mutual discussions with the successful bidder.

#### **K) Statutory Variation:**

Any statutory increase in the taxes and duties subsequent to bidder's offer, if it takes place within the original contractual delivery date, will be borne by IISc, Bangalore subject to the claim being supported by documentary evidence. However, if any decrease takes place the advantage will have to be passed on to IISc, Bangalore.



## L) Disputes and Jurisdiction:

Any legal disputes arising out of any breach of contract pertaining to this tender shall be settled in the court of competent jurisdiction located within the city of Bangalore, India.

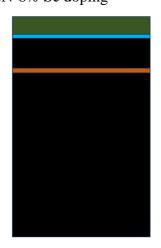
### M) General:

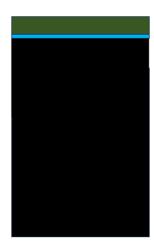
- 1. All amendments, time extension, clarifications etc., within the period of submission of the tender will be communicated electronically. No extension in the bid due date/time shall be considered on account of delay in receipt of any document(s) by mail.
- 2. The bidder may furnish any additional information, which is necessary to establish capabilities to successfully complete the envisaged work. It is however, advised not to furnish superfluous information.
- 3. Any information furnished by the bidder found to be incorrect, either immediately or at a later date, would render the bidder liable to be debarred from tendering/taking up of work in IISc, Bangalore.
- 4. Technical datasheet (CoA) includes detail on RCA process & Bow/Warp measurement method on bare Silicon and after thermal oxide carried out in cleanroom.
- 5. Manufacturer CoC must be attached.



## <u>Section 4 - Technical Requirements of thin-film Piezoelectric (AlN/AlScN)</u> <u>deposited on Silicon and SOI wafers</u>

Stack Configuration: Thin-film piezoelectric (AlN /AlScN) on Molybdenum (bottom electrode) on SOI or Silicon AlScN-8% Sc doping





AlN or AlScN Molybdenum Oxide Silicon

The vendor can use a seed layer if required.

| Wafer Spec                             | Quantity |  |
|--|----------|--|
| Wafer Type 1:                          | 4 Nos.   |  |
|  |          |  |
| Thin-film deposition                   |          |  |
| Thickness of AlN: $0.9 \pm 0.1 \mu m$  |          |  |
| Thickness of Mo: $0.15 \pm 0.05 \mu m$ |          |  |
|  |          |  |
| SOI configuration                      |          |  |
|  |          |  |
| 100mm SOI WAFERS                       |          |  |
| DEVICE TOP LAYER:                      |          |  |
| Type/Dopant: Intrinsic/Undoped         |          |  |
| Orientation: $(1-0-0)\pm0.5^{\circ}$   |          |  |
| Resistivity: ≥100 ohm-cm               |          |  |
| Thickness: 15±0.5µm                    |          |  |
| Finish: Frontside Polished             |          |  |
| BURIED THERMAL OXIDE:                  |          |  |
| Thickness: 2µm±5%                      |          |  |
| HANDLE LAYER:                          |          |  |



| Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm |        |
|--|--------|
| Wafer #2:  | 4 Nos. |
| Thin-film deposition Thickness of AlN: $1.5 \pm 0.1 \mu m$   |        |
| Thickness of Mo: $0.15 \pm 0.05 \mu m$   |        |
| SOI configuration  |        |
| 100mm SOI WAFERS   |        |
| DEVICE TOP LAYER:  |        |
| Type/Dopant: Intrinsic/Undoped   |        |
| Orientation: (1-0-0)±0.5°  |        |
| Resistivity: ≥100 ohm-cm<br>Thickness: 15±0.5µm  |        |
| Finish: Frontside Polished   |        |
| BURIED THERMAL OXIDE:  |        |
| Thickness: 2µm±5%  |        |
| HANDLE LAYER:  |        |
| Diameter: 100±0.5mm  |        |
| Type/Dopant: N/Ph  |        |
| Orientation: $(1-0-0)\pm0.5^{\circ}$   |        |
| Resistivity: 1-20 ohm-cm   |        |
| Thickness: 450±25um  |        |
| Flat: Semi Standard  |        |
| Finish: Backside Polished  |        |
| Overall wafer:   |        |
| Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm   |        |
| 20 π ππα _υφμ  |        |
|  |        |



| Wafer #3:   | 4 Nos. |
|---|--------|
| Thin-film deposition                                  |        |
| Thickness of AlScN: 0.9 ± 0.1 μm                      |        |
| Thickness of Mo: $0.15 \pm 0.05 \mu\text{m}$          |        |
| SOI configuration                                     |        |
| 100mm SOI WAFERS                                      |        |
| DEVICE TOP LAYER:                                     |        |
| Type/Dopant: Intrinsic/Undoped                        |        |
| Orientation: $(1-0-0)\pm0.5^{\circ}$                  |        |
| Resistivity: ≥100 ohm-cm                              |        |
| Thickness: 15±0.5μm                                   |        |
| Finish: Frontside Polished                            |        |
| BURIED THERMAL OXIDE:                                 |        |
| Thickness: 2µm±5%                                     |        |
| HANDLE LAYER:   |        |
| Diameter: 100±0.5mm                                   |        |
| Type/Dopant: N/Ph                                     |        |
| Orientation: (1-0-0)±0.5°<br>Resistivity: 1-20 ohm-cm |        |
| Thickness: 450±25um                                   |        |
| Flat: Semi Standard                                   |        |
| Finish: Backside Polished                             |        |
| Overall wafer:  |        |
| Edge Exclusion≤5mm, TTV≤5µm,                          |        |
| BOW/WARP≤50μm   |        |
|   |        |
|   |        |
| Wafer #4:   | 4 Nos. |
|   |        |
| Thin-film deposition                                  |        |
| Thickness of AlScN: $1.5 \pm 0.1 \mu m$               |        |
| Thickness of Mo: $0.15 \pm 0.05 \mu m$                |        |
| ·   |        |
| SOI configurations                                    |        |
|   |        |
| 100mm SOI WAFERS                                      |        |
| DEVICE TOP LAYER:                                     |        |
| Type/Dopant: Intrinsic/Undoped                        |        |

Assistant Professor

www.cense.iisc.ac.in/gayathri-pillai



Orientation:  $(1-0-0)\pm0.5^{\circ}$ Resistivity: ≥100 ohm-cm Thickness: 15±0.5µm Finish: Frontside Polished **BURIED THERMAL OXIDE:** Thickness: 2µm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation:  $(1-0-0)\pm0.5^{\circ}$ Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5µm, BOW/WARP≤50µm Wafer #5 5 Nos. Thin-film deposition Thickness of AlScN:  $0.9 \pm 0.1 \mu m$ Thickness of Mo:  $0.15 \pm 0.05 \,\mu m$ **SOI** configurations 100mm SOI WAFERS DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation:  $(1-0-0)\pm0.5^{\circ}$ Resistivity: ≥100 ohm-cm Thickness: 40±0.5µm Finish: Frontside Polished **BURIED THERMAL OXIDE:** Thickness: 2µm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation:  $(1-0-0)\pm0.5^{\circ}$ Resistivity: 1-20 ohm-cm Thickness: 450±25um



| Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #6  5 Nos.  Thin-film deposition  Thickness of AIN: 0.9 ± 0.1 μm Thickness of Mo: 0.15 ± 0.05 μm  SOI configurations  100mm SOI WAFERS DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos. | Flat: Semi Standard                     |         |
|---|---|---------|
| Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #6  Thin-film deposition  Thickness of AlN: 0.9 ± 0.1 μm Thickness of Mo: 0.15 ± 0.05 μm  SOI configurations  100mm SOI WAFERS DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  | Finish: Backside Polished               |         |
| Wafer #6  Thin-film deposition  Thickness of AlN: 0.9 ± 0.1 μm Thickness of Mo: 0.15 ± 0.05 μm  SOI configurations  100mm SOI WAFERS DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  | Overall wafer:                          |         |
| Wafer #6  Thin-film deposition  Thickness of AlN: 0.9 ± 0.1 μm Thickness of Mo: 0.15 ± 0.05 μm  SOI configurations  100mm SOI WAFERS DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  | Edge Exclusion≤5mm, TTV≤5µm,            |         |
| Wafer #6  Thin-film deposition  Thickness of AlN: 0.9 ± 0.1 μm Thickness of Mo: 0.15 ± 0.05 μm  SOI configurations  100mm SOI WAFERS DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  | ·                                       |         |
| Thin-film deposition  Thickness of AlN: 0.9 ± 0.1 μm Thickness of Mo: 0.15 ± 0.05 μm  SOI configurations  100mm SOI WAFERS DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  | ·                                       |         |
| Thickness of AlN: 0.9 ± 0.1 μm Thickness of Mo: 0.15 ± 0.05 μm  SOI configurations  100mm SOI WAFERS DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  | Wafer #6                                | 5 Nos.  |
| Thickness of AlN: 0.9 ± 0.1 μm Thickness of Mo: 0.15 ± 0.05 μm  SOI configurations  100mm SOI WAFERS DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  |   |         |
| Thickness of Mo: 0.15 ± 0.05 μm  SOI configurations  100mm SOI WAFERS DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.   | Thin-film deposition                    |         |
| Thickness of Mo: 0.15 ± 0.05 μm  SOI configurations  100mm SOI WAFERS DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.   |   |         |
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| 100mm SOI WAFERS DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  | Thickness of Mo: $0.15 \pm 0.05 \mu m$  |         |
| 100mm SOI WAFERS DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  |   |         |
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| DEVICE TOP LAYER: Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.   | 100 GOLWAFEDG                           |         |
| Type/Dopant: Intrinsic/Undoped Orientation: (1-0-0)±0.5° Resistivity: ≥100 ohm-cm Thickness: 40±0.5μm Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.   |   |         |
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| Finish: Frontside Polished BURIED THERMAL OXIDE: Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.   |   |         |
| BURIED THERMAL OXIDE: Thickness: 2µm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5µm, BOW/WARP≤50µm  Wafer #7  3 Nos.  | •                                       |         |
| Thickness: 2μm±5% HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  |   |         |
| HANDLE LAYER: Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  |   |         |
| Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  | · ·                                     |         |
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| Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  |   |         |
| Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  | * * *                                   |         |
| Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.   | · · · · · · · · · · · · · · · · · · ·   |         |
| Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.   | •                                       |         |
| Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.   |   |         |
| Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.   |   |         |
| Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm  Wafer #7  3 Nos.  |   |         |
| BOW/WARP≤50μm  Wafer #7  3 Nos.   |   |         |
| Wafer #7 3 Nos.   |   |         |
|   | BOW/WARP≤30μm                           |         |
|   | Wafer #7                                | 3 Nos   |
| Thin-film deposition  | , , arer 117                            | 0.1100. |
| Thin-film deposition  |   |         |
| 1   | Thin-film deposition                    |         |
|   | 1                                       |         |
| Thickness of AlScN: $0.9 \pm 0.1 \mu m$   | Thickness of AlScN: $0.9 \pm 0.1 \mu m$ |         |



| Thickness of Mo: $0.15 \pm 0.05 \mu m$   |        |
|--|--------|
| Silicon wafer configuration  |        |
| 100mm Si WAFER   |        |
| BURIED THERMAL OXIDE: Thickness: 2μm±5% Diameter: 100±0.5mm Type/Dopant: N/Ph Orientation: (1-0-0)±0.5° Resistivity: 1-20 ohm-cm Thickness: 450±25um Flat: Semi Standard Finish: Backside Polished Overall wafer: Edge Exclusion≤5mm, TTV≤5μm, BOW/WARP≤50μm |        |
| Wafer #8   | 3 Nos. |
| Thin-film deposition   |        |
| Thickness of AlN: $0.9 \pm 0.1 \mu m$<br>Thickness of Mo: $0.15 \pm 0.05 \mu m$  |        |
| Silicon Wafer configuration  |        |
|  |        |
| 100mm Si WAFER   |        |



• Stress of piezoelectric thin film must be <150MPa across the wafer.

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- Thickness deviation of the metal and piezoelectric thin film should be less than 0.5% across the wafer.
- FWHM of the AlN piezoelectric thin film must be <1.25 degree and AlScN piezoelectric thin film must be <1.5 degree.
- The magnitude of d33 of AlN >4.5pC/N and for AlScN it must be >7pC/N.
- Loss tangent of piezoelectric material must be at 1kHz < 0.02.
- The vendor should have the capability to map stress across the wafer.
- The vendor should have the capability to do XRD of the wafer.
- The Si and SOI vendor should provide wafer specification certification.
- The spare wafers (due to MOQ-10 constraint) on which no thin film deposition has been performed should be shipped along with the AlN/AlScN wafers.

The vendor should provide references of their customers who have used their thin-film deposition facilities to realize MEMS devices (RF MEMS, sensors, and actuators).

**Qualification:** The XRD of the wafers will be conducted at CeNSE, IISc and it should match the quality claimed by the vendor. Thickness cross-section will be verified using SEM.



## **Section 5 - Technical Bid**

The technical bid should furnish all requirements of the tender along with all annexures in this section and submitted to

The Chairperson, Attn: Dr. Gayathri Pillai Centre for Nano Science and Engineering Indian Institute of Science Bangalore – 560012, India



# Annexure-1: Details of the Bidder

The bidder must provide the following mandatory information & attach supporting documents wherever mentioned:

Details of the Bidder

| Sl. | No | Items | Details | S |
|-----|----|-------|---------|---|
|     |    |       |         |   |

- 1. Name of the Bidder
- 2. Nature of Bidder (Attach attested copy of

Certificate of Incorporation/ Partnership Deed)

- 3. Registration No/ Trade License, (attach attested copy)
- 4. Registered Office Address
- 5. Address for communication
- 6. Contact person- Name and Designation
- 7. Telephone No
- 8. Email ID
- 9. Website
- 10. PAN No. (attach copy)
- 11. GST No. (attach copy)

| Signature of the Bidder |       |
|-------------------------|-------|
|                         |       |
| Name                    |       |
| Designation, Seal       | Date: |



# Annexure-2: Declaration regarding experience

To, The Chairperson, Centre for Nanoscience and Engineering, Indian Institute of Science, Bangalore – 560012, India

Ref: Tender No: XXXXXXXXX

Dated: XXXXX

Supply of thin-film Piezoelectric (AlN/AlScN) deposited on Metallized Silicon and SOI wafers, CeNSE, IISc Bangalore.

Sir,

I've carefully gone through the Terms & Conditions contained in the above referred tender. I hereby declare that my company / firm has ---- years of experience in supplying and installing ------

(Signature of the Bidder) Printed Name Designation, Seal Date:



# Annexure-3: Declaration regarding track record

To,
The Chairperson,
Centre for Nano Science and Engineering
Indian Institute of Science,
Bangalore – 560012, India

Ref: Tender No: XXXXXXX

Dated: XXXXX

Supply of thin-film Piezoelectric (AlN/AlScN) deposited on Metallized Silicon and SOI wafers, CeNSE, IISc Bangalore.

Sir.

I've carefully gone through the Terms & Conditions contained in the above referred tender. I hereby declare that my company/ firm is not currently debarred / blacklisted by any Government / Semi Government organizations / institutions in India or abroad. I further certify that I'm competent officer in my company / firm to make this declaration.

Or

I declare the following
Sl.No Country in which the
company is Debarred
/blacklisted / case is
Pending Blacklisted / debarred by
Government / Semi
Government/Organizations
/Institutions
ReasonSince when and

ReasonSince when and

for how long

(NOTE: In case the company / firm was blacklisted previously, please provide the details regarding period for which the company / firm was blacklisted and the reason/s for the same).

Yours faithfully (Signature of the Bidder) Name Designation, Seal



Date:

# Annexure – 4: Declaration for acceptance of terms and conditions

To,
The Chairperson,
Centre for Nano Science and Engineering
Indian Institute of Science,
Bangalore – 560012, India

Ref: Tender No: XXXXXX

Dated: XXXX

Supply of thin-film Piezoelectric (AlN/AlScN) deposited on Metallized Silicon and SOI wafers, CeNSE, IISc Bangalore.

Sir,

I've carefully gone through the Terms & Conditions as mentioned in the above referred tender document. I declare that all the provisions of this tender document are acceptable to my company. I further certify that I'm an authorized signatory of my company and am, therefore, competent to make this declaration.

Yours faithfully,

(Signature of the Bidder) Name Designation, Seal

Date:



## Annexure – 5: Details of items quoted:

- a. Company Name
- b. Product Name
- c. Part / Catalogue number
- d. Product description / main features
- e. Detailed technical specifications
- f. Remarks

#### Instructions to bidders:

- 1. Bidder should provide technical specifications of the quoted product/s in detail.
- 2. Bidder should attach product brochures along with technical bid.
- 3. Bidders should clearly indicate compliance or non-compliance of the technical specifications provided in the tender document.



## Section 6 - Commercial Bid

The commercial bid should be furnished with all requirements of the tender with supporting documents as mentioned under:

| S.No<br>1.<br>1.a<br>1.b  | Essential item  | Cat. Number s noted in the to essential items) | echnical specif | Unit Price ication | Sub total |
|---|---|--|-----------------|--------------------|-----------|
| 2.<br>2.a<br>2.b  | Optional items noted in the technical specification (details of essential items)                          |  |                 |                    |           |
| 3.<br>4.  | Accessories for operation and installation<br>All Consumables, spares and software to be supplied locally |  |                 |                    |           |
| 5.<br>6.  | Warranty (1 years) AMC 2 years beyond warranty  |  |                 |                    |           |
| Any additional items S.No Description Cat. Number Quantity Unit Price Sub total |   |  |                 |                    |           |

### Addressed to

The Chairperson, Attn: Dr. Gayathri Pillai Centre for Nano Science and Engineering Indian Institute of Science Bangalore – 560012, India



## Section 7 - Checklist

(This should be enclosed with technical bid- Part A)
The following items must be checked before the Bid is submitted:

- 1. Sealed Envelope "A": Technical Bid
- 1. Section 5- Technical Bid (each page signed by the authorized signatory and sealed) with the below annexures:
- a. Annexure 1: Bidders details
- b. Annexure 2: Declaration regarding experience
- c. Annexure 3: Declaration regarding clean track record
- d. Annexure 4: Declaration for acceptance of terms and conditions
- e. Annexure 5: Details of items quoted
- 2. Copy of this tender document duly signed by the authorized signatory on every page and sealed.
- 2. Sealed Envelop "B": Commercial Bid Section 6: Commercial Bid

Your quotation must be submitted in two envelopes: Technical Bid (Envelope A) and Commercial Bid (Envelope B) super scribing on both the envelopes with Tender No. and due date and both of these in sealed covers and put in a bigger cover which should also be sealed and duly super scribed with Tender No., Tender description & Due Date.

Thanking you, Gayathri Pillai Assistant Professor Centre for Nano Science and Engineering Indian Institute of Science, Bangalore, India 560012.

Office: +91-80-2293-3250 E-mail: gpillai@iisc.ac.in